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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ZAMAN, FAISAL M	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,858	KAUSHIK ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 16-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-27 and 31-34* is/are allowed.

6)☒ Claim(s) *1-5,7-10,28,29,35 and 37* is/are rejected.

7)☒ Claim(s) *6,30,36 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 30 November 2005 regarding the rejection to Claims 1-5, 7-10, and 28-29 as being anticipated by Bealkowski et al. ("Bealkowski") (U.S. Patent No. 6,282,596) under 35 USC 102(e) have been fully considered but they are not persuasive.

Regarding Applicant's argument to the rejection to Claims 1 and 5, see pages 14 and 15, the examiner has established that a communication interface on the hot plug module is inherent, since the hot plug module is coupled to CPU connectors 14. The examiner believes that Bealkowski et al. teaching supplying power along with a clock signal to a processor card 11a-11d (which inherently comprises of a communication interface, see Applicant's argument, page 14, lines 19-22) once a processor card is couple to the system bus 18 is equivalent to enabling the communication interface on the processor card.

Regarding Applicant's argument to the rejection of Claims 2-4, see page 15, Bealkowski discloses enabling a communication interface (Figure 3, item 14a-d) of the running computing device (Column 3, lines 27-29) that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device (Figure 4, Column 7 line 51 – Column 8 line 30).

Regarding Applicant's argument to the rejection of Claim 5, see page 16, Bealkowski teaches memory caching processors, see Column 4, lines 3-6.

Regarding Applicant's argument to the rejection of Claims 7 and 8, see pages 17 and 18, Bealkowski teaches adding memory from a hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to processes in Column 9, lines 42-45. Bealkowski teaches that the processor caches are flushed to remove the work load from the processor of the hot plug module.

Regarding Applicant's argument to the rejection of Claim 28, see page 22, since Bealkowski teaches enabling a communication interface on the hot plug module to establish a communication link with the running computing device, as described above in the discussion of Claim 1, Bealkowski similarly teaches the limitation "the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device".

2. Applicant's arguments filed 30 November 2005 regarding the rejection to Claims 1 and 7-9 as being anticipated by Olarig et al. ("Olarig") (U.S. Patent No. 6,587,909) under 35 USC 102(e) have been fully considered but they are not persuasive. Olarig teaches enabling a communication interface on a hot plug module to establish a communication link with a running computing device, see Column 6, lines 50-57, specifically where Olarig recites "circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal".

3. Applicant's arguments, see pages 13-23, filed 30 November 2005, with respect to Claims 6, 16-23, 24-27, 30, and 31-34 as being anticipated by Bealkowski under 35

USC 102(e) have been fully considered and are persuasive. The rejection of 4 October 2005 regarding these claims has been withdrawn.

Claim Objections

3. Claim 7 is objected to because of the following informalities:

In line 3, "running computing device; " (the word "and" was removed in the amendment) should be --running computing device; **and**"--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1 and 7-9** are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig et al. ("Olarig") (U.S. Patent No. 6,587,909).

As for claim 8, Olarig teaches a method of adding memory to a running computing device (see figure 1, computer system 10, memory modules 14 and column 6 lines 50-57, wherein additional memory modules are added by hot-plugging to the computer system 10), comprising:

Identifying memory of a hot plug module in response to the hot plug module being physically coupled to the running computing device (see column 5 lines 1-23, wherein the System Control Interrupt (SCI) generates interrupt to the ACPI driver for "hot add" memory event. The ACPI driver responds to the "hot add" memory event by performing the 5 tasks, wherein the first task is to determine if memory has been added or removed and if the has been added, determine whether if it is a "hot addition" or a "hot replacement". This task is equivalent to what is claimed by identifying a memory module, which is being added or removed from the computer system 10. Furthermore, tasks 2-5 performing the memory configuration for the "hot add" memory event).

Adding the identifying memory to the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to threads (see column 3 lines 15-20, wherein the memory modules are added to the computer system as claimed), and

Enabling a communication interface on the hot plug module to establish a communication link with the running computing device (see column 5 lines 1-23, wherein the 5 tasks performing the configuration for establishing communication between the newly added memory module and the computer system 10).

As for claims 1, 7 and 9, Olarig teaches a method of adding one or more caching agents to a running computing device (see figure 1, memory modules 14, computer system 10), comprising:

Identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device (see column 5 lines 1-23, wherein the System Control Interrupt (SCI) generates interrupt to the ACPI driver for "hot add" memory event. The ACPI driver responds to the "hot add" memory event by performing the 5 tasks, wherein the first task is to determine if memory has been added or removed and if the has been added, determine whether if it is a "hot addition" or a "hot replacement". This task is equivalent to what is claimed by identifying a memory module, which is being added or removed from the computer system 10. Furthermore, tasks 2-5 performing the memory configuration for the "hot add" memory event).

Adding the identified caching agents of the hot plug module to a resource pool of the running computing device (see column 3 lines 15-20, wherein the memory modules are added to the computer system as claimed).

Enabling communication interface on the hot plug module to establish a communication link with the running computing device (see column 5 lines 1-23, wherein the 5 tasks performing the configuration for establishing communication between the newly added memory module and the computer system 10).

Claim Rejections - 35 USC § 102

6. **Claims 1-5, 7-10, 28-29, 35, and 37** are rejected under 35 U.S.C. 102(e) as being anticipated by Bealkowski et al. ("Bealkowski") (U.S. Patent No. 6,282,596).

As for claims 1 and 8, Bealkowski teaches a method of adding one or more caching agents to a running computing device (see figure 1-3, hot plug processor cards 11, 20, 30 and column 3 lines 9-11, column 4 lines 4-11, wherein each processor card is hot plug and each processor card comprises a cache), comprising identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device (see figure 4 and column 7 line 51 to column 8 line 31, wherein each processor is identified with an agent ID and the hot plug controller uses the agent ID identify which processor card is removed or inserted to the computer system); and adding the identified caching agents of the hot plug module to a resource pool of the running computing device (see figure 2, service processor 31 and column 5 lines 31-60, wherein the service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine. Further, column 3 lines 35-41, teaches integrated processor cards which including cache into the data processing. Therefore, the caches of the processor cards are considered adding memory to the data processing as well); and enabling a communication interface on the hot plug module to establish a communication link with the running computing device (see figures 1-3, processor cards 11, 20, 30 are hot plugged to the data processing system 10 via the CPU connectors. Further, data processing system 10 supports hot plugging and initializing processor cards for communication between the newly added processor card and the processing system 10 via the CPU connectors as discloses in column 3 lines 1-15 and lines 35-41).

As for claims 2 and 9, Bealkowski further teaches comprising enabling a communication interface (Figure 3, item 14a-d) of the running computing device (Column 3, lines 27-29) that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device (see figure 4, wherein the flow chart describes the processor for establishing communication between the processor cards and the computer system; Column 7 line 51 – Column 8 line 30).

As for claims 3 and 10, Bealkowski teaches performing a self test of the hot plug module, and in response to passing the self test, enabling the communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device (see column 8 lines 31-39).

As for claim 4, Bealkowski teaches initializing the hot plug module, and after initializing the hot plug module, enabling the communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device (see column 9 lines 10 lines 4-10).

As for claim 5, Bealkowski teaches wherein adding comprises adding one or more memory caching processors of the identified caching agents to a processor pool of the running system (see column 5 lines 53-60 and Column 4, lines 3-6).

As for claim 7, Bealkowski teaches identifying memory of the hot plug module in response to the hot plug module being physically coupled to the running computing device; and adding the identified memory of the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to processes (see Column 9, lines 42-45).

As for claim 28, Bealkowski teaches a computing device comprising, a midplane comprising a coupler and a hot plug interface to track a state associated with the coupler (see figure 1); a hot plug module comprising a coupler to detachably couple the hot plug module to the coupler of the midplane and resources coupled to the coupler of the hot plug module via a hot plug interface of the hot plug module (see figure 1, processor cards are connected to the CPU connectors 14 to the system bus 18), the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device (see column 5 lines 41-52); and a processor coupled to the hot plug interface of the midplane (see figure 1, service processor 31), the processor to add the resources to the computing device without rebooting in response to determining that the hot plug interface of the midplane indicates the resources are ready to join (see column 1 lines 57-58).

As for claim 29, Bealkowski teaches wherein the midplane comprises a hot plug monitor that provides the hot plug interface of the midplane with a signal indicative of

whether the coupler of the hot plug module has been coupled to the coupler of the midplane, and the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane (see column 8 lines 1-5).

As for claims 35 and 37, Bealkowski teaches transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system to establish the communication link (Figure 4, Column 7 line 51 – Column 8 line 65; ie. the various communications between the processor card [the hot plug module] and the system bus through CPU connectors 14 [power-on configuration, BIST, determination of AP/BSP, etc.] indicate that data packets are transferred between the communication interface on the hot plug module and the communication interface of the running computing system, since the use of data packets in communicating information in a computing system was well known in the art at the time of the invention).

Allowable Subject Matter

7. **Claims 6, 30, 36, and 38** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. **Claims 16-27, and 31-34** are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 6, the prior art of record, either alone or in combination, does not teach the method of Claim 1 wherein adding comprises adding one or more *memory caching input/output hubs* of the identified agents to an input/output pool of the running system.

Regarding Claim 30, the prior art of record, either alone or in combination, does not teach the computing device of Claim 28, wherein the processor programs the hot plug interface of the midplane to generate a hot plug interrupt *in response to a change in receipt of framing packets*.

Regarding Claims 36 and 38, the prior art of record, either alone or in combination, does not teach the method of Claim 3 and 9, respectively, further comprising determining that the communication link has been established in response to transferring *a predetermined number of error free packets* between the communication interface on the hot plug module and the communication interface of the running computer system.

Regarding independent Claims 16, 24, and 31, the prior art of record, either alone or in combination, does not teach examining a *plurality of interface control registers* in response to a hot plug event, and identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers.

Prior Art of Record

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Johnson et al. (U.S. Patent No. 5,781,744) discloses a method and apparatus for ensuring safe peripheral connection. Egan et al. (U.S. Patent No. 5,875,308) discloses a peripheral component interconnect (PCI) architecture having hot-plugging capability for a data-processing system. Huang et al. (U.S. Patent No. 6,131,134) discloses a hot plug-and-play converter of a universal serial bus interface. Chen et al. (U.S. Patent No. 6,591,324) discloses a hot swap processor card and bus. Matsunaga (U.S. Patent No. 6,742,055) discloses a data transmission system, data transmission terminal, controller and interface method. Scarpino (U.S. Patent No. 6,748,496) discloses a method and apparatus for providing cacheable data to a peripheral device.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

fmz

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/16/06